UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/787,413	02/27/2004	Yukihiro Urakawa	249344US2SDIV	4542

22850 7590 04/20/2006

OBLON, SPIVAK, MCCLELLAND, MAIER & NEUSTADT, P.C.
1940 DUKE STREET
ALEXANDRIA, VA 22314

EXAMINER	
ABRAHAM, FETSUM	

ART UNIT	PAPER NUMBER
2826	

DATE MAILED: 04/20/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/787,413	URAKAWA, YUKIHIRO	
	Examiner	Art Unit	
	Fetsum Abraham	2826	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *10/27/05*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *the rest* is/are rejected.

7)☒ Claim(s) *4 and 12* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claim 1 states the following:

A COC device comprising: a logic chip having a logic circuit; a memory chip mounted on the logic chip, the memory chip comprising: basic chips functioning as a chip independently from each other; and a dicing line interposed between the basic chips, connecting the basic chips, and configuring a part of the memory chip; and a bump connecting the logic chip and the memory chip.

Claims 1,4,7-10,12,16,17,20 are rejected under 35 U.S.C. 103(a) as being unpatentable over Nagao (6,677,674) in view of Kimura et al (6,078,096) and further in view of Kim et al (6,594,818).

As for claims 1,7, the primary reference discloses the claimed COC package in fig. 7A where a memory chip (21) is mounted on logic chip (20) and both secured with each other with bump bonding means (2), a generic memory

wafer having memory units separated by scribe lanes. Clearly, the two distinct chips are connected to one another by bump connecting means.

The primary reference disclose most of the subject matters claimed but may have missed to indicate to detail how the chips were separated from each other. However, Kimura et al teach that chips were separated from the mother wafer and each other by dicing means. The DRAM chips separated by the claimed means are capable working independent of each other so far as their relation ship with the controller is concerned. Clearly, memory can be expanded by increasing the number of memory chips in a given system configuration. But neither does it mean that they cannot function independent of each other, nor does it mean they were interdependent.

The secondary reference specifically establishes the following in the abstract:

a) that DRAM chips are adjacent to one another in a common wafer and each constitute 4 MB DRAM chips. The description establishes the fact that the DRAM chips are individually standing elements in the wafer.

b) an interconnection between the chips is said to be provided at the dicing lines level of the chips in the wafer. The chips are indeed connected to one another through "short-circuit protecting circuit".

Therefore, it would have been obvious to one skilled in the art to separate chips in a wafer by scribing lines and interconnect the chips by wires formed in the scribing lines since the methodology provides a better solution to circuit

density induced problems compared to structures having circuits on other parts of the wafer away from the scribe lines.

Although it is conceptually clear that the DRAM chips have the capacity to function independent of each other while still in a matrix, the prior arts may have been silent about the notoriously known subject matter. However, Kim et al fills the conceptual gap by teaching that mutually exclusive memory chips of different capacity can be extracted from unit chips formed in common mother wafer (see abstract). Therefore, it would have been obvious to one skilled in the art to separate unit cells in singularity or multiplicity based on desired memory capacity since the practice satisfies various memory size and capacity requirement of different memory systems in different devices.

As for said configuring a part of the memory chip, the functional language is dependent on memory size required for a given application scenario. Independent DRAMs are known to be configured so to satisfy memory requirement in a system. Therefore, the claimed functional language is common to all memory matrices.

As for claims 2,10, the chips in the last two patents are similar units.

As for claims 8,9, the logic circuits supporting the memory chips in the primary reference is capable of generating control signals that assign word and data bits that in turn change word bits as understood by the examiner but called by the applicant as “organization”

As for claims 4,12, **"product by process"** claims are directed to the product per se, no matter how actually made, In re Hirao, 190 USPQ 15 at 17

(footnote 3). See also In re Brown, 173 USPQ 685 and In re Thorpe, 227 USPQ 964, 966. Therefore, the way the product was made does not carry any patentable weight as long as the claims are directed to a device. Further, note that the applicant has the burden of proof in such cases, as the above case law makes clear. Also see MPEP 2113.

As for claim 16, the primary art is a SiP (System in Package) device because it packages two different chips in integration.

As for claim 17, figure 2 of the primary reference shows that the COC structure is well packaged and the chips covered with encapsulant material and a container that contains the overall system.

As for claims 20, flush memories are DRAMs and the prior arts apply to all types of DRAMs.

Claims 5,6,13,14,15,18,19 are rejected under 35 U.S.C. 103(a) as being unpatentable over Nagao (6,677,674) in view of Kimura et al (6,078,096) and further in view of Kim et al (6,594,818) and further in view of Majima (4,408,875).

As for claims 5,13, although the shape of memory chips and length are known to be variable in the art and the specification indicates the arbitrary nature of the chosen size (see page 22, 18-20), the prior arts are silent on their chip shapes and length. However, Majima discloses a square memory chip having an area of 10 mm**2 (see column 2, 5-15). Therefore, it would have been obvious to one skilled in the art to form the claimed memory shape because they tend to be simpler for projector-type exposure processing and the selected length because high-precision exposure has limitations as chip sizes go smaller and smaller.

As for claims 6,14, dicing line width is inversely proportional to yield. It is a known function of the target number of chips yielded from a given wafer. Therefore, it is known to be variable in the art. The claimed width by itself is not patentable unless criticality is an issue. In this case, the specification contains no disclosure of either the critical nature of the claimed arrangement or any unexpected results arising therefrom. Where patentability is said to be based upon particular chosen dimensions or upon another variable recited in a claim, the applicant must show that the chosen dimensions are critical. In re Woodruff, 919 F.2d 1575, 1578, 16 USPQ2d 1934, 1936 (Fed. Cir. 1990). In fact, in pages 22 and 23, the width seems to have been picked arbitrarily and no teaching exists of its critical nature (see the last paragraph of page 23).

Claims 3 and 11 have been objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

As for claim 18, all memory chips work with preplanned WORD organization.

As for claims 19, flush memories are DRAMs and the prior arts apply to all types of DRAMs.

Claims 4,12 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

THIS ACTION IS MADE FINAL. Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Examiner's answer to applicant's argument

Applicant's argument that only one type of memory chip is cut from the wafer has been considered but found to be contradictory with the claims in the application. To be specific, the following cases in point are provided.

Claims 1,9 only require independent functionality of the claimed chips, which DRAMs have.

Claim 2,5,10,11,13 in fact establish chip physical similarity in very clear manner.

Claim 19 in fact tells that the subject matter of the claimed invention was directed towards DRAM chips only.

The argument is therefore found to be moot.

As for claiming dicing line is missing from Kimura's patent is unacceptable because dicing and lining are mutually inclusive. The claim language concerning "dicing line" is fully met by Kimura.

Please note that the examiner disagrees with the notion that the there had been modification of the patents to challenge the claimed invention.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Fetsum Abraham whose telephone number is: 571-272-1911. The examiner can normally be reached on 8:00 - 18:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Nathan J Flynn can be reached on 571-272-1915.

Fetsum Abraham
3/23/06